WHAT IS CLAIMED IS:

1. An apparatus comprising:

a functional unit configured to perform an operation on one or more block operands;

an accumulator memory comprising a first memory bank having a first interface and a second memory bank having a second interface, wherein the first and second interfaces are independent of each other; and

a control unit configured to receive a first command to perform the operation on a first operand identified by an address of the accumulator memory and to store a first result of the operation to the same address;

wherein in response to receiving the first command, the control unit is configured to cause the first memory bank to output the first operand to the functional unit via the first interface and to cause the second memory bank to store the first result generated by the functional unit via the second interface.

2. The apparatus of claim 1, wherein in response to the functional unit completing the first operation, the control unit is configured to cause the second memory bank to provide a second operand if the control unit receives a second command that identifies the second operand using the address.

3. The apparatus of claim 1, wherein the control unit is further configured to receive a second command to perform the operation on a second operand and to store a second result of the operation to the address, wherein in response to receiving the second command, the control unit is configured to cause the second memory bank to provide the

second operand to the functional unit via the second interface and to cause the first memory bank to store the second result via the first interface.

4. The apparatus of claim 3, wherein in response to the functional unit completing the second operation, the control unit is configured to cause the first memory bank to provide a third operand if the control unit receives a third command that identifies the third operand using the address.

5. The apparatus of claim 1, wherein the operation has a duration extending from when the operation is initiated to when the operation completes, and wherein for the duration of the operation that is performed on the first operand, the first memory bank is in a providing mode and the second memory bank is in a storing mode.

6. The apparatus of claim 1, wherein the operation comprises a parity calculation, and wherein the command is issued by a storage system controller.

7. The apparatus of claim 1, wherein the control unit is configured to restart the operation in response to an error occurring by providing the first operand from the first memory bank again and by storing the result of the restarted operation in the second memory bank.

8. The apparatus of claim 7, wherein the error comprises a functional unit error that occurs while performing the operation.

9. The apparatus of claim 7, wherein the functional unit is configured to perform the operation on two operands, and wherein the error comprises a transmission error that occurs while a second operand is being provided from a source other than the first and second memory banks.

10. The apparatus of claim 1, wherein the functional unit is configured to perform the operation on two operands, wherein the second operand is provided by a source other than the first and second memory banks.

11. The apparatus of claim 10, wherein the source and the accumulator memory each comprise a same type and speed of memory.

12. An apparatus comprising:

a functional unit configured to perform an operation on one or more block operands;

an accumulator memory comprising a first memory bank having a first interface and a second memory bank having a second interface, wherein the first and second interfaces are independent of each other; and

a control unit configured to receive commands to perform the operation, wherein each command to perform the operation instructs the control unit to perform the operation on an operand identified by a first address in the accumulator memory and to store a result of the operation to a second address in the accumulator memory;

wherein in response to every command to perform the operation that the control unit receives, the control unit is configured to provide the operand from one of the first and second memory banks to the functional unit and to map the second address to a location in the other one of the first and second memory banks so that the result of the operation is always stored in a different memory bank than the operand is stored in.

13. The apparatus of claim 12, wherein the first and second addresses are the same.

14. The apparatus of claim 12, wherein the operation comprises a parity calculation, and wherein the command is issued by a storage system controller.

15. The apparatus of claim 12, wherein the functional unit is configured to perform the operation on two operands, wherein one of the operands is provided by either the first or the second memory bank and the other operand is provided by a source other than the first and second memory banks.

16. The apparatus of claim 15, wherein the source and the accumulator memory each comprise a same type and speed of memory.

17. The apparatus of claim 12, wherein during the performance of the operation initiated by receiving one of the commands, the control unit is configured to restart the operation in response to an error occurring by providing the operand from the one of the first and second memory banks again.

18. The apparatus of claim 17, wherein the error comprises a functional unit error that occurs while performing the operation.

19. The apparatus of claim 17, wherein the functional unit is configured to perform the operation on two operands, wherein one of the operands is provided by either the first or the second memory bank and the other operand is provided by a source other than the first and second memory banks, and wherein the error comprises a transmission error that occurs while the second operand is being provided from the source.

20. The apparatus of claim 17, wherein the operation has a duration extending from when the operation is initiated to when the operation completes, and wherein for the duration of the operation that is performed on a first operand, the first memory bank is in a providing mode and the second memory bank is in a storing mode.

21. A method of performing a block operation, the method comprising:

receiving a first command to perform an operation on a first operand identified by a first address and to store a first result of the operation to the first address; and

in response to said receiving a first command:

providing the first operand from a first memory bank in an accumulator memory via a first interface;

performing the operation on the first operand; and

storing the first result of the operation in a second memory bank in the accumulator memory via a second interface, wherein the first and second interface are independent of each other.

22. The method of claim 21, further comprising causing the second memory bank to provide a second operand in response to receiving another command that identifies the second operand using the first address after said storing the first result of the operation in the second memory bank.

23. The method of claim 21, further comprising:

receiving a second command to perform the operation on a second operand identified by the first address and to store a second result of the operation to the first address; and

in response to said receiving a second command:

providing the second operand from the second memory bank via the second interface;

performing the operation on the second operand; and

storing the second result in the first memory bank via the first interface.

24. The method of claim 23, further comprising causing the first memory bank to provide a third operand in response to receiving another command that identifies the third operand using the first address after said storing the second result of the operation in the first memory bank.

25. The method of claim 21, wherein the operation has a duration extending from when the operation is initiated to when the operation completes, and wherein for the duration of the operation that is performed on the first operand, the first memory bank is in a providing mode and the second memory bank is in a storing mode.

26. The method of claim 21, wherein the operation comprises a parity calculation, and wherein the first command is issued by a storage system controller.

27. The method of claim 21, wherein said performing the operation on the first operand comprises performing the operation on both the first operand and another operand, wherein the other operand is provided by a source other than the first and second memory banks.

28. The method of claim 27, wherein the accumulator memory and the source each comprise a same type and speed of memory.

29. The method of claim 21, further comprising restarting said performing the operation on the first operand in response to an error occurring, wherein said restarting comprises providing the first operand from the first memory bank again and storing the result of the restarted operation in the second memory bank.

30. The method of claim 29, wherein the error comprises an error that occurs while performing the operation.

31. The method of claim 29, wherein the error comprises a transmission error that occurs while another operand is being provided by a source other than the first and second memory banks.

32. A method of performing a block operation, the method comprising:

receiving one or more commands to perform an operation on an operand identified by a first address in an accumulator memory and to store a result of the operation to a second address in the accumulator memory, wherein the accumulator memory comprises two independently interfaced memory banks; and

in response to receiving each of the one or more commands:

providing the operand from one of memory banks in the accumulator memory;

performing the operation on the operand; and

mapping the second address to a new address in the other one of the memory banks in the accumulator memory so that the result of the

operation is always stored in a different memory bank than the operand is stored in.

33. The method of claim 32, wherein the first and second addresses are the same.

34. The method of claim 32, wherein the operation comprises a parity calculation, and wherein the command is issued by a storage system controller.

35. The method of claim 32, wherein said performing the operation on the operand comprises performing the operation on a first operand provided by the accumulator memory and another operand provided by a source other than the accumulator memory.

36. The method of claim 35, wherein the accumulator memory and the source each comprise a same type and speed of memory.

37. The method of claim 32, further comprising restarting said performing the operation on a first operand in response to an error occurring, wherein said restarting comprises providing the first operand from a first memory bank again and storing the result of the restarted operation in a second memory bank.

38. The method of claim 37, wherein the error comprises a transmission error that occurs while another operand for the operation is being provided from a source other than the accumulator memory.

39. The method of claim 37, wherein the error comprises a functional unit error that occurs while performing the operation.